REMARKS

Claims 1-4, 7-11 and 14-22 are pending in the present application. Claims 1, 3, 4, 7-10, 14 and 15 have been amended. Claims 16-22 have been presented herewith. Claims 5, 6, 12 and 13 have been canceled.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

The Examiner is respectfully requested to confirm that the drawings as filed along with the Response to Notice To File Corrected Application Papers dated April 9, 2004, are acceptable.

Information Disclosure Statement

The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement filed on August 17, 2005, and to confirm that the documents listed therein have been considered and will be cited of record in the present application.

Claim Rejections-35 U.S.C. 102

Claims 1, 2, 4, 5, 9, 11 and 12 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Sato et al reference (Japanese Patent Publication No. 2002-64055). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 1 includes in combination a substrate which has a main surface; an alignment mark "which is formed on the main surface and which has a pattern, wherein the pattern in a plane view has a shape that is obtained by eliminating corners from a polygon"; and an oxidation prevention cover film "on the alignment mark and formed as having the pattern". Applicant respectfully submits that the Sato et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that the Sato et al. reference shows a cover film 76 formed over the metal film to prevent oxidation of the metal film. However, as described beginning in paragraph [0087] of the English translation of the Sato et al. reference, Figs. 7 and 8 illustrate sequential production process steps of a semiconductor device, wherein photoresist 74 is used as a mask to etch silicon oxide layer 73 formed on substrate 70. As described in paragraph [0089], a first layer aluminum wiring 75 is subsequently formed on silicon oxide 73, as shown in Fig. 7(b). Thereafter as described in paragraph [0090], silicon oxide layer 76 is formed to cover first layer aluminum wiring 75, as shown in Fig. 7(c). Processing of the semiconductor

device is subsequently completed as described with respect to Fig. 8(b) in paragraph [0092], wherein second layer aluminum wiring 78 is connected to first layer aluminum wiring 75 through a contact hole.

Accordingly, Figs. 7 and 8 of the Sato et al. reference as relied upon by the Examiner, illustrate manufacturing processing steps of a semiconductor device including first and second layer aluminum wirings 75 and 78. An alignment mark is not specifically described with respect to the structures as illustrated in Figs. 7 and 8 of the Sato et al. reference.

In contrast, the English language abstract of the Sato et al. reference describes marks 41 and 42 formed on wafer 1, as further described in paragraphs [0029] through [0032] and paragraphs [0038] through to [0041] of the English translation with respect to Figs. 1 and 2. Various other alignment marks are described. However, the Sato et al. reference does not appear to specifically describe the alignment marks as having an oxidation prevention cover film formed thereon. More particularly, the Sato et al. reference does not appear to specifically describe an oxidation prevention cover film on an alignment mark that is formed as having the pattern of the alignment mark, as would be necessary to meet the features of claim 1.

Applicant emphasizes that the semiconductor device in Figs. 7 and 8 of the Sato et al. reference is not particularly described as including an alignment mark, and thus does not disclose an oxidation prevention cover film formed on an alignment mark and having the pattern of the alignment mark. Moreover, silicon oxide 76 in Figs. 7 and 8 of

the Sato et al. reference is not particularly described as an oxidation prevention cover film. Accordingly, Applicant respectfully submits that the semiconductor device of claim 1 distinguishes over the Sato et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1, 2, and 4 is improper for at least these reasons.

The semiconductor device of claim 9 includes in combination a substrate; an alignment mark; and an oxidation prevention cover film "on the alignment mark and formed as having the first through fourth sub-patterns".

As emphasized previously, the Sato et al. reference as relied upon by the Examiner does not specifically disclose an oxidation prevention cover film on an alignment mark. More particularly, the Sato et al. reference does not disclose an oxidation prevention cover film on an alignment mark and formed as having first through fourth sub-patterns of the alignment mark. Applicant therefore respectfully submits that the semiconductor device of claim 9 distinguishes over the the Sato et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 9 and 11, is improper for at least somewhat similar reasons as set forth above with respect to claim 1.

Claim Rejections-35 U.S.C. 103

Claims 3, 6-8, 10 and 13-15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sato et al. reference. This rejection is respectfully traversed for

the following reasons.

Regarding claims 3 and 10, the Examiner has asserted that the specification fails to provide teachings about the criticality of the pattern thickness of the alignment mark. However, as described beginning on page 16, line 17 of the present application, forming the pattern widths of the alignment mark in a range of 0.6 μm to 0.8 μm makes it possible to bury the trenches by metal, and to thus eliminate the stepped shape of the alignment mark. As further described beginning on page 17, line 4 of the application, a pattern width smaller than 0.6 μm interferes with measurement accuracy at the time of performing alignment and measurement, and a pattern width of 0.8 μm or more requires increasing the thickness of the tungsten film at the time of chemical vapor deposition. Accordingly, contrary to the Examiner's assertion, the criticality of the thickness is set forth in the specification.

Applicant respectfully submits that the prior art as specifically relied upon by the Examiner does not appear to disclose or even remotely suggest pattern width of alignment marks in a range of 0.6 μm to 0.8 μm, as featured in claims 3 and 10. Applicant therefore respectfully submits that claims 3 and 10 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection of claims 3 and 10 is improper for at least these additional reasons.

Regarding claims 8 and 15, the Examiner has alleged that it would have been obvious to make the cover film of iridium based metal, "since it has been held to be within the general skill of a worker in the art to select a known material on the basis of

its suitability for the intended use as a matter of obvious design choice". However, the oxidation prevention cover film of the invention is specifically used to prevent oxidation of the alignment mark. The Sato et al. reference as relied upon by the Examiner does not appear to specifically show a cover film on the alignment mark, and also does not appear to disclose or suggest the desirability of preventing oxidation of the alignment mark. Accordingly, in absence of specifically relied upon prior art showing the need to prevent oxidation of an alignment mark, the Examiner's assertion that the use of an iridium based metal oxide prevention cover film on an alignment mark would have been obvious, appears to be based merely on impermissible hindsight. Applicant therefore respectfully submits that claims 8 and 15 would not have been obvious in view of the prior art as relied upon by the Examiner for at least these additional reasons.

Claims 16-22

The semiconductor device of claim 16 includes in combination a substrate; an alignment mark "on the main surface of the substrate, wherein the alignment mark is strip-like and has the shape of a polygon without corners along a plane parallel to the main surface of the substrate"; and an oxidation prevention cover film "on the alignment mark, wherein the oxidation prevention cover film is strip-like and has annular shape along another plane parallel to the main surface of the substrate".

Applicant respectfully submits that the Sato et al. reference as relied upon by the Examiner does not specifically disclose an oxidation prevention cover film formed on an

alignment mark, particularly wherein the oxidation prevention cover film is strip-like and has annular shape. Accordingly, Applicant respectfully submits that claims 16-22 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

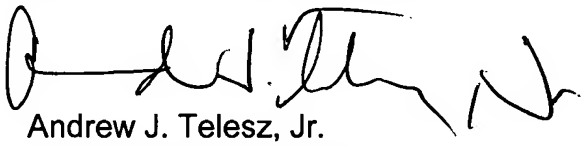
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to November 29, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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